

FIG. 6A

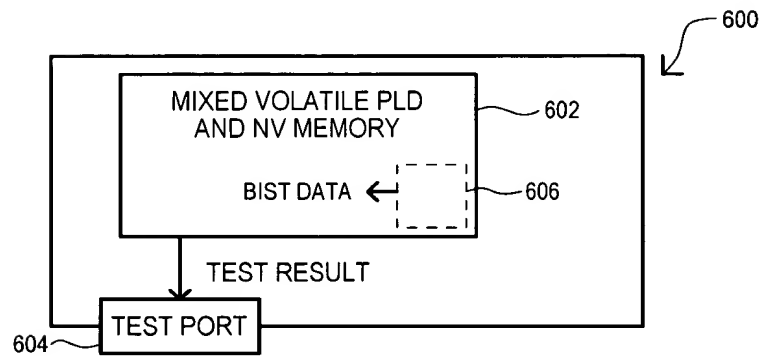


FIG. 6B

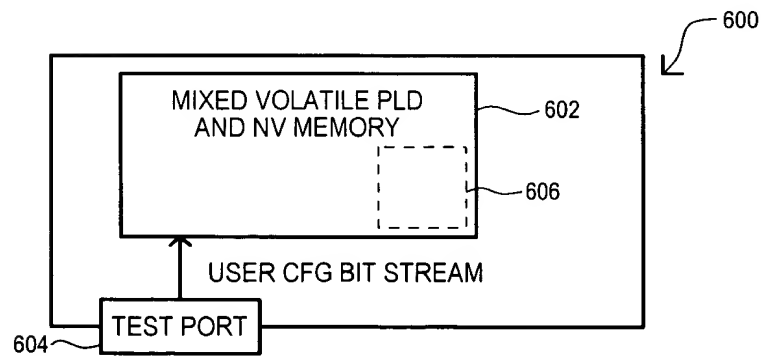


FIG. 6C

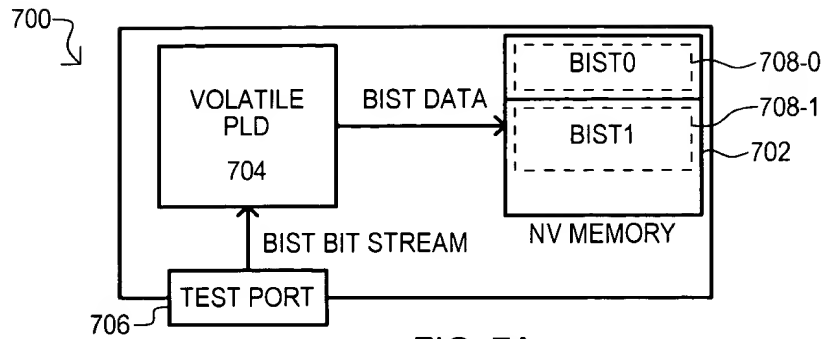


FIG. 7A

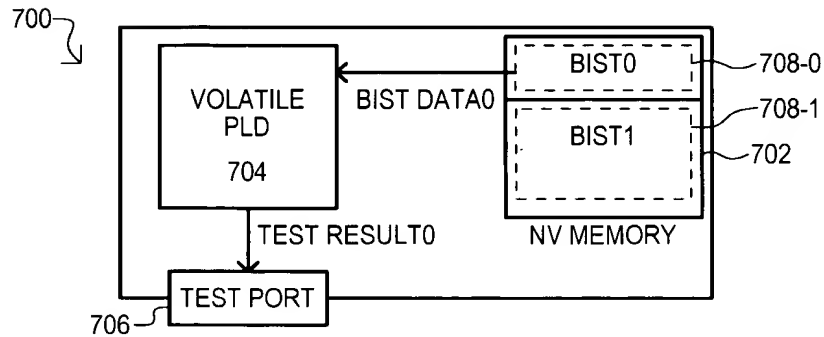


FIG. 7B

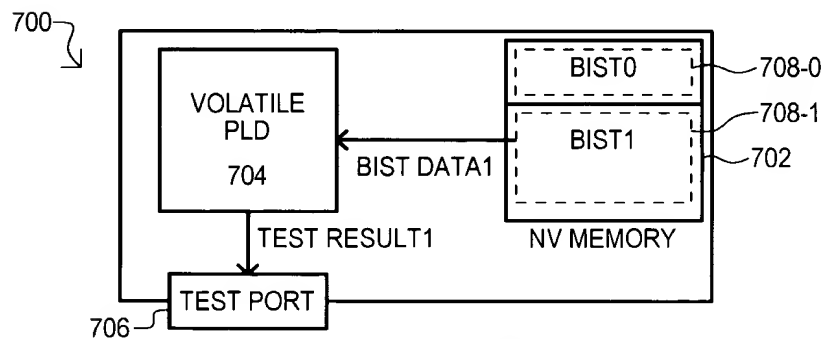


FIG. 7C

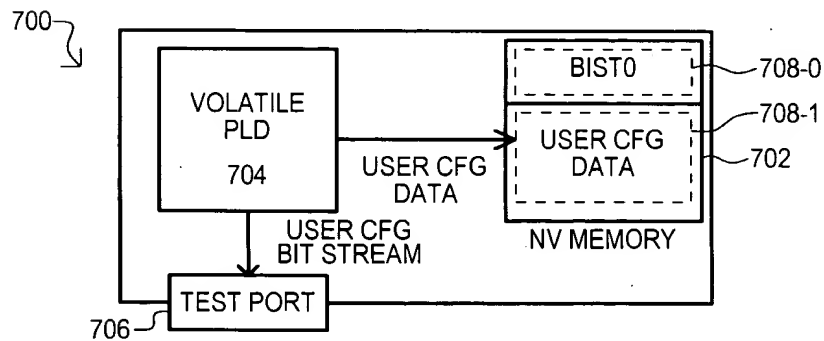


FIG. 7D

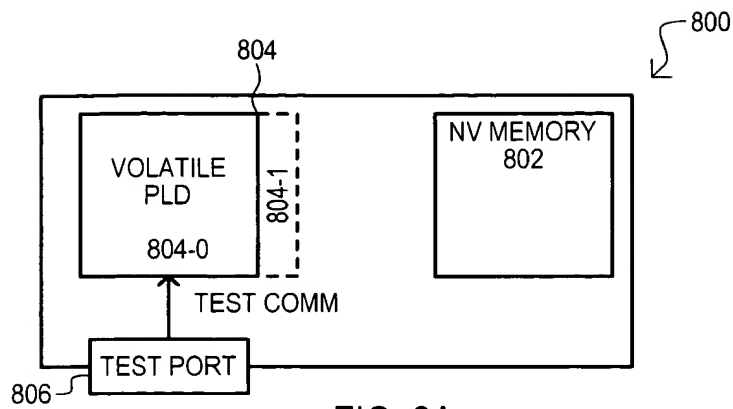


FIG. 8A

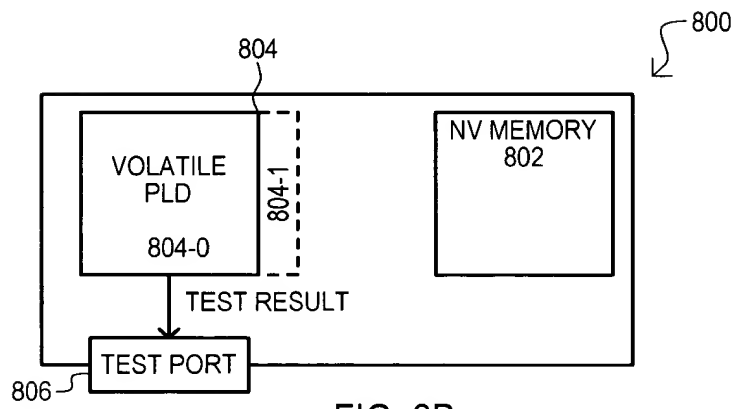


FIG. 8B

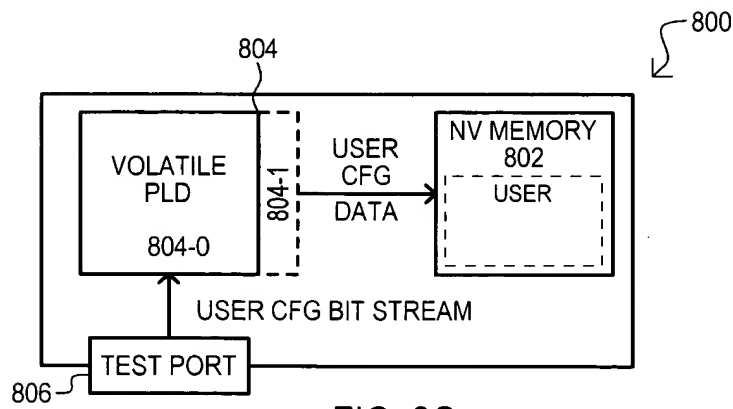


FIG. 8C

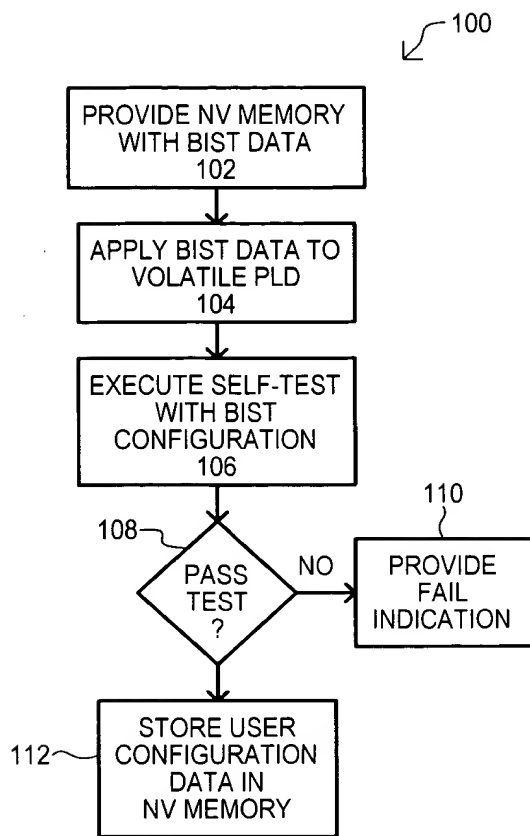
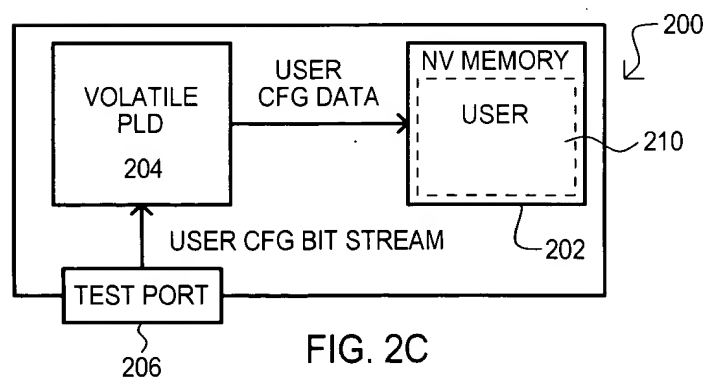


FIG. 1

FIG. 2A is a block diagram of a BIST system. A TEST PORT (206) is connected to a VOLATILE PLD (204) and an NV MEMORY (202). The VOLATILE PLD (204) outputs BIST DATA to the NV MEMORY (202). The NV MEMORY (202) contains a BIST block (208). A BIST BIT STREAM is also shown as an output from the system.

FIG. 2B



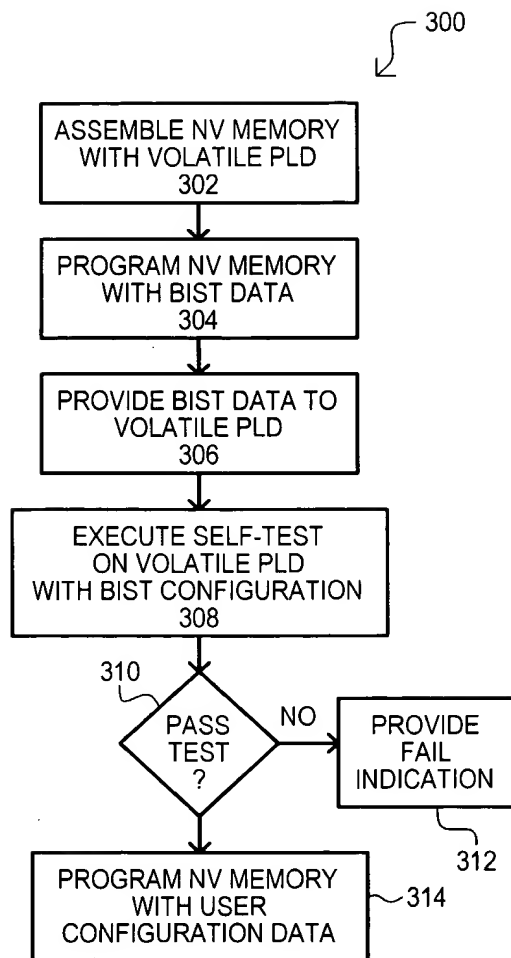
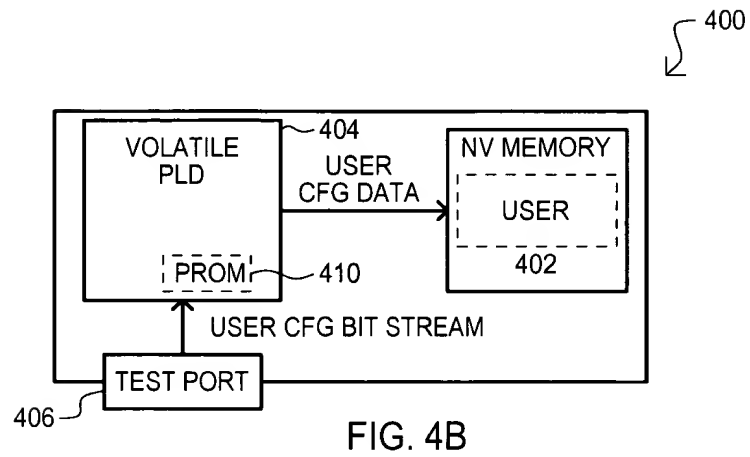
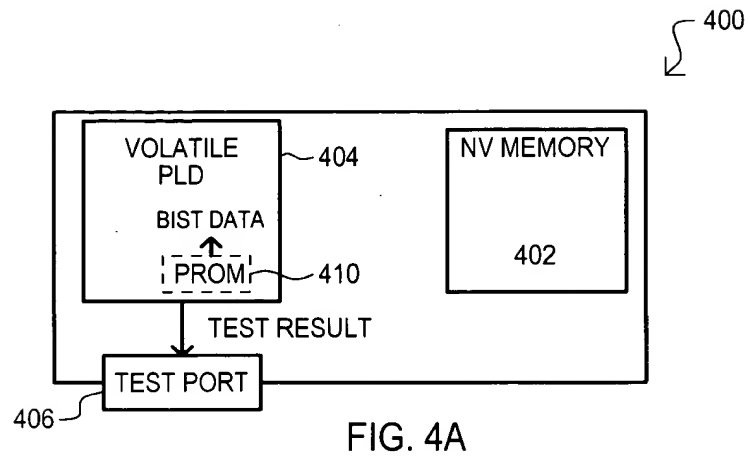


FIG. 3



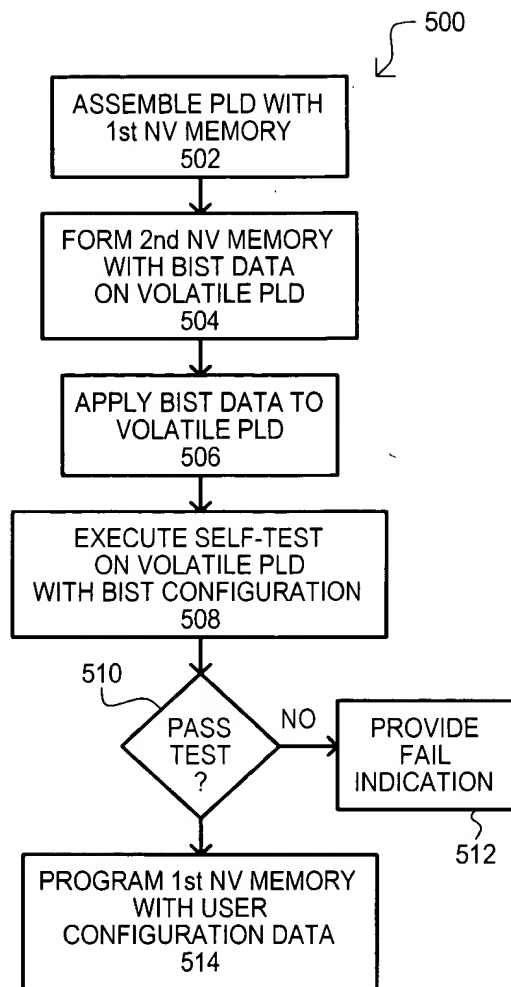


FIG. 5